

1. An electrical signal regenerator comprising an equalizer and a clock data recovery circuit and a switch, said switch being operable to either connect the data recovery circuit to the output when an input signal of a higher bitrate multiplex signal is detected or to bypass the data recovery circuit and connect the equalizer to the output when an input signal of a lower bitrate multiplex signal is detected.
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2. An electrical signal regenerator according to claim 1, wherein the clock data recovery circuit comprises a detector for detecting the bitrate of the input signal.
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3. An electrical signal regenerator according to claim 1 comprising a delimiter for deciding upon logical signal value 0 or 1.
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4. An electrical signal regenerator according to claim 1, comprising a test loop controllably connectable from the output to the input of the regenerator.
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5. An electrical signal regenerator according to claim 1, wherein said equalizer being an analogue equalizer comprising a tapped delay line.
6. An electrical signal regenerator according to claim 1, wherein said equalizer being an analogue equalizer comprising a first tap and a second

tap, the first tap having a higher delay than the second tap, both taps being connected to a adder-subtractor for generating a difference signal.

7. An electrical signal regenerator according to claim 6, wherein the signal 5 ration between the two taps is adjustable.

8. An electrical signal regenerator according to claim 6, wherein the signal 10 ration between the two taps is adjustable, and wherein the ration is determined by two peak detectors.

9. A network element, comprising internal electrical signal paths, wherein at 15 least part of said paths are terminated by an electrical signal regenerator comprising an equalize and a clock data recovery circuit and a switch, said switch being operable to either connect the data recovery circuit to an output when an input signal of a higher bitrate multiplex signal is detected or to bypass the data recovery circuit and connect the equalizer to the output when an input signal of a lower bitrate multiplex signal is detected.

10. A network element according to claim 9 being an optical crossconnect 20 comprising an electrical space switching matrix, said matrix comprising a number of switch modules being interconnected by means of internal electrical cables, an electrical signal regenerator is coupled to one end of each internal electrical cable in front of a switching module.

11. A network element according to claim 10, wherein said matrix modules 25 being adapted to output a test signal at each unused output port and wherein the electrical signal regenerators are adapted to raise an alarm when neither a test signal nor a valid input signal is detected.

12. A method of transmitting an electrical signal having either a first or a 30 second bitrate, wherein the first bitrate is higher than the second bitrate, said method comprising the steps of
- transmitting said electrical signal via a signal path;
- detecting the bitrate of said electrical signal received from the signal path;

- in the case the electrical signal has the first bitrate, performing a first regeneration of said electrical signal and then performing a second regeneration and
- in the case the signal has the second bitrate, performing said first regeneration of said signal, only.

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13. A method according to claim 12, wherein said first signal regeneration is an electrical equalization and wherein said second signal regeneration is a clock data recovery.